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Sheet 1 of 4

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Application Number	09/312,302
Filing Date	05/14/1999
First Named Inventor	Mario Nemirovsky
Art Unit	2154
Examiner Name	Larry Donaghue
Attorney Docket Number	P3803

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5600837 A *	02-04-1997	Artieri, Alain	RECEIVED OCT 27 2003 Technology Center 2100
		US- 5461722 A *	10-24-1995	Goto, Tatuhiro	
		US- 5542088 A	07-30-1996	Jennings, Jr. et al.	
		US- 5748468 A	05-05-1998	Notenboom et al.	
		US- 5745778 A	04-28-1998	Alfieri, Robert	
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		US- 5713038 A	01-27-1998	Motomura, Masato	
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		US- 5561776 B1	10-01-1996	Popescu et al.	

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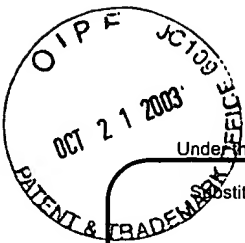
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		US- 6535905 B1	03-18-2003	Kalafatis et al.	
		US- 4200927 A	04-29-1998	Hughes et al.	
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		US- 6016542 A	01-18-2000	Gottlieb et al.	
		US- 5361337 A	11-01-1994	Okin, Kenneth	
		US- 6308261 B1	10-23-2001	Morris et al.	
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		US- 5815733 A *	09-29-1998	Anderson et al.	
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		US- 6052708 A *	04-18-2000	Flynn et al.	
		US- 6212544 B1 *	04-03-2001	Borkenhagen et al.	
		US- 5546593 A *	08-13-1996	Kimura et al.	
		US- 5913049 A *	06-15-1999	Shiell et al.	
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NON PATENT LITERATURE DOCUMENTS

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g		* FISKE et al., "Thread Prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors", 1995, pp 210 -221, IEEE	
g		* YAMAMOTO, Wayne, "An Analysis of Multistreamed, Superscalar Processor Architectures", University of California Santa Barbara dissertation, December 1995, Santa Barbara, US	
g		* STEERE et al., "A Feedback - Driven Proportion Allocator for Real-Rate Scheduling", Third Symposium on Operating Systems Design and Implementation, February 1999, pp 145-158, USENIX Association	
g		* YAMAMOTO et al., "Increasing Superscalar Performance Through Multistreaming", 1995	
g		* TULLSEN et al., "Simultaneous Multithreading: Maximizing on-Chip Parallelism", 22nd Annual International Symposium on Computer Architecture, June 1995, Santa Margherita Ligure, Italy	
g		YOAZ et al., "Speculation Techniques for Improving Load Related Instruction Scheduling", 1999, pp 42-53, IEEE	
g		KESSLER, R.E., "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 Mhz", August 1998	
g		TULLSEN et al., "Supporting Fine-Grained Synchronization on a Simultaneous Multithreading Processor", 5th Annual International Symposium on Computer Architecture, January 1999	
g		NEMIROVSKY et al., "Quantitative Study of Data Caches on a Multistreamed Architecture", Workshop on Multithreaded Execution Architecture and Compilation, January 1998	
g		LI et al., "Design and Implementation of a Multiple-Instruction-Stream Multiple-Execution-Pipeline Architecture", 7th International Conference on Parallel and Distributed Computing and Systems, October 1995, Washington D.C.	

Examiner Signature	Date Considered	
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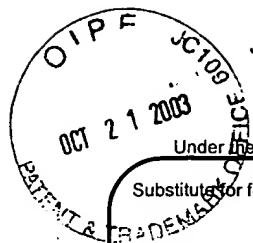
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10		Donalson et al., "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance", 26th Hawaii Conference on Systems Sciences, 1993, pp 448-456, vol. 1	

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